METHODS FOR REMOVING DOPED POLYSILICON FROM MICROFEATURE WORKPIECES

TECHNICAL FIELD

[0001] The present invention relates to methods and apparatuses for removing doped silicon material from microfeature workpieces.

BACKGROUND

[0002] Mechanical and chemical-mechanical planarization processes (collectively, "CMP") remove material from the surfaces of micro-device workpieces in the production of microelectronic devices and other products. Figure 1 schematically illustrates a rotary CMP machine 10 with a platen 20, a carrier head 30, and a polishing pad 40. The CMP machine 10 may also have an under-pad 25 between an upper surface 22 of the platen 20 and a lower surface of the polishing pad 40. A drive assembly 26 rotates the platen 20 (as indicated by arrow F) and/or reciprocates the platen 20 back and forth (as indicated by arrow G). Because the polishing pad 40 is attached to the under-pad 25, the polishing pad 40 moves with the platen 20 during planarization.

[0003] The carrier head 30 has a lower surface 32 to which a microfeature workpiece 50 may be attached, or the workpiece 50 may be attached to a resilient pad 34 under the lower surface 32. The carrier head 30 may be a weighted, free-floating wafer carrier, or an actuator assembly 36 may be attached to the carrier head 30 to impart rotational motion (as indicated by arrow J) and/or reciprocal motion (as indicated by arrow I) to the microfeature workpiece 50.

[0004] The polishing pad 40 and a polishing solution 60 define a polishing or planarizing medium that mechanically and/or chemically-mechanically removes

material from the surface of the microfeature workpiece 50. The polishing solution 60 may be a conventional CMP slurry with abrasive particles and chemicals that etch and/or oxidize the surface of the microfeature workpiece 50, or the polishing solution 60 may be a "clean" nonabrasive solution without abrasive particles. In most CMP applications, abrasive slurries with abrasive particles are used on non-abrasive polishing pads, and clean non-abrasive solutions without abrasive particles are used on fixed-abrasive polishing pads.

[0005] To planarize the microfeature workpiece 50 with the CMP machine 10, the carrier head 30 presses the workpiece 50 facedown against the polishing pad 40. More specifically, the carrier head 30 generally presses the microfeature workpiece 50 against the polishing solution 60 on a polishing surface 42 of the polishing pad 40, and the platen 20 and/or the carrier head 30 moves to rub the workpiece 50 against the polishing surface 42. As the microfeature workpiece 50 rubs against the polishing surface 42, the polishing medium removes material from the face of the workpiece 50.

[0006] During many of the CMP processes conducted to form a typical microfeature workpiece, it is necessary to stop the material removal process at a selected plane of the microfeature workpiece 50. Accordingly, existing processes include disposing a stop layer at the selected plane in the microfeature workpiece 50. The chemical makeup of the polishing solution 60 is then chosen to (a) preferentially remove material overlaying the stop layer, and (b) stop removing material from the workpiece 50 when the stop layer is exposed. For example, polysilicon has been proposed as a stop layer material when positioned adjacent to an oxide layer, and one proposed polishing solution 60 includes a non-ionic surfactant that selectively removes the oxide and then stops the material removal upon exposing the underlying polysilicon stop layer. Further details of methods and solutions for carrying out such a process are disclosed in an article titled "Effects Of Non-Ionic Surfactants On Oxide-To-Polysilicon Selectively During Chemical Mechanical Polishing," (Lee et al., *J. of the Electrochemical Society*, June 17, 2002) incorporated herein in its entirety by reference.

[0007] Polysilicon has other functions in a typical microfeature workpiece 50. For example, many conventional microfeature workpieces 50 include doped polysilicon as a component for forming conductive and/or semiconductive microelectronic structures. One problem associated with conventional methods for planarizing doped polysilicon is that such methods tend to leave defects in the planarized polysilicon surface. These defects can include holes, pits, divots, or other non-uniformities that adversely affect the performance of the conductive via or other structure formed from the polysilicon. One approach to addressing this problem is to reduce the level of doping in the polysilicon. A drawback with this approach is that it can adversely affect the conductivity of the polysilicon, and therefore the performance of devices formed from the polysilicon. Another approach to addressing this drawback is to adjust some process conditions at which the polysilicon is deposited on the microfeature workpiece 50. A drawback with this approach is that it can increase the time required to complete the deposition process and can accordingly increase the cost of producing devices from the microfeature workpiece 50.

BRIEF DESCRIPTION OF THE DRAWINGS

[0008] Figure 1 is a partially schematic, cross-sectional side view of a portion of a rotary planarizing machine in accordance with the prior art.

[0009] Figure 2 is a partially schematic cross-sectional side elevational view of a portion of a polishing apparatus positioned to remove material from a microfeature workpiece in accordance with an embodiment of the invention.

[0010] Figure 3 is a partially schematic cross-sectional illustration of an arrangement for disposing a second polishing liquid adjacent to a microfeature workpiece in accordance with an embodiment of the invention.

[0011] Figure 4 is a partially schematic cross-sectional illustration of a microfeature workpiece after having a layer of doped silicon material removed.

[0012] Figure 5 is a partially schematic illustration of an arrangement of multiple planarizing apparatuses for removing doped silicon from microfeature workpieces.

DETAILED DESCRIPTION

A. Introduction

[0013] The present invention is directed toward methods and apparatuses for removing doped polysilicon from microfeature workpieces. The term "microfeature workpiece" is used throughout to include a workpiece formed from a substrate upon which and/or in which submicron circuits or components, and/or data storage elements or layers are fabricated. Submicron features in the substrate include but are not limited to trenches, vias, lines, and holes. These features typically have a submicron width (e.g., ranging from, for example, 0.1 micron to 0.75 micron) generally transverse to a major surface (e.g., a front side or a back side) of the workpiece. The term "microfeature workpiece" is also used to include a substrate upon which and/or in which micromechanical features are formed. Such features include read/write head features and other micromechanical features having submicron or supramicron dimensions. In any of these embodiments, the workpiece substrate is formed from suitable materials, including ceramics, and may support layers and/or other formations of other materials, including but not limited to metals, dielectric materials and photoresists.

[0014] A method for removing material from a microfeature workpiece in accordance with one aspect of the invention includes contacting a polishing pad material with a portion of a microfeature workpiece having a doped silicon material. The method can further include disposing a polishing liquid between the doped silicon material and the polishing pad material, with the polishing liquid including a surfactant. At least one of the microfeature workpiece and the polishing pad material is moved relative to the other while the microfeature workpiece contacts the polishing pad material and the polishing liquid. The method can further include simultaneously and uniformly removing at least some of the doped silicon material from regions of the microfeature workpiece having different crystalinities and/or different doping characteristics by contacting the

doped silicon material with a surfactant in the polishing liquid as at least one of the microfeature workpiece and the polishing material moves relative to the other.

[0015] In further aspects of the invention, the surfactant can be selected to include a generally non-ionic surfactant, and/or the polishing liquid can include from about 0.001% to about 1.0% surfactant by weight. In still further aspects of the invention, the method can include disposing a first polishing liquid between the doped silicon material and the polishing pad material for removing at least some of the doped silicon material at a first rate, and disposing a second polishing liquid (having a surfactant) between the doped silicon material and the polishing pad material to remove at least some of the doped silicon material at a second rate slower than the first rate. The second polishing liquid can be formed by disposing a surfactant in the first polishing liquid, or it can be separately disposed on the polishing pad material. In still a further aspect of the invention, the microfeature workpiece can be moved from one polishing pad material (having the first polishing liquid) to another polishing pad material (having the second polishing liquid) during processing.

B. Methods and Apparatuses for Removing Doped Polysilicon

[0016] Figure 2 is a partially schematic illustration of a portion of an apparatus 110 configured to remove material from a microfeature workpiece 150 (a portion of which is shown in Figure 2) in accordance with an embodiment of the invention. In one aspect of this embodiment, the apparatus 110 can include a platen 120 and an underpad 125 that support a polishing pad 140. The polishing pad 140 can have a polishing pad surface 142 that carries a first polishing liquid 160a. In one embodiment, the polishing pad 140 can be a fixed abrasive polishing pad having fixed abrasive elements disposed in the pad itself. The first polishing liquid 160a can accordingly include cutting fluid. In another embodiment, the first polishing liquid 160a can include a suspension of abrasive elements. In either embodiment, the polishing pad 140 and the first polishing liquid 160a can define a polishing medium for removing material from the microfeature workpiece 150, for example, during a planarizing process. The microfeature workpiece 150 can be

supported by a carrier (not shown in Figure 2) as it contacts the polishing medium. The carrier and/or the polishing pad 140 can move relative to each other in a manner generally similar to that described above to remove material from the microfeature workpiece 150.

[0017] In one aspect of an embodiment shown in Figure 2, the microfeature workpiece 150 can include a substrate material 151 (e.g., an oxide glass) having a substrate material surface 152. The microfeature workpiece 150 can further include an aperture 153 extending from the substrate material surface 152. A doped silicon material 154 can be disposed in the aperture 153 and can extend over the substrate material surface 152 adjacent to the aperture 153. In one embodiment, the doped silicon material 154 can form a via to electrically connect features within or on the substrate material 151. In other embodiments, the doped silicon material 154 can form other structures. In a particular embodiment, the doped silicon material 154 can be negatively doped with substances such as phosphorous. In other embodiments, the doped polysilicon material 154 can be positively doped with substances such as boron.

[0018] In one embodiment, the doped silicon material 154 includes doped amorphous silicon, which is polished and heat treated to form doped polycrystalline silicon (or doped polysilicon). Accordingly, the term "doped silicon" includes both doped amorphous silicon and doped polysilicon. The processes described below as being performed on doped silicon materials and/or doped silicon portions can be performed on doped silicon and/or doped polysilicon.

[0019] In a further aspect of an embodiment shown in Figure 2, the microfeature workpiece 150 can include an intermediate layer 155 between the substrate material surface 152 and the portion of the doped silicon material 154 disposed outwardly from the aperture 153. The intermediate layer 155 can include an anti-reflective coating, a stop layer, or another type of layer. In still further embodiments, the intermediate layer 155 can be eliminated.

[0020] During polishing, the excess doped silicon material 154 external to the aperture 153 can be removed as the microfeature workpiece 150 rubs against the polishing pad material 140 in the presence of the first polishing liquid 160a. In one embodiment, the material removal process can be conducted at a temperature of up to about 125° F, and in other embodiments, the process can be conducted at other temperatures. In one embodiment, the first polishing liquid 160a can include a commercially available slurry, for example, an alkaline, silica slurry available from Rodel of Newark, Delaware. In other embodiments, the first polishing liquid 160a can have other compositions.

[0021] Referring now to Figure 3, the first polishing liquid 160a can form defects 156 in the doped silicon material 154. These defects 156 can include, but are not limited to, holes, pits, and/or divots. It is believed that the presence of such defects may be correlated with dopant-rich zones or regions of the doped silicon material 154, and/or regions of the doped silicon material 154 having increased levels of crystal order, and/or regions of the doped silicon material 154 having different crystal orientations. It is further believed that the foregoing conditions can lead to preferentially higher etch rates in some regions of the doped silicon material 154 than in others, which can in turn cause the formation of the defects 156. Accordingly, in one embodiment of the invention, a second polishing liquid 160b is disposed between the polishing pad 140 and the doped silicon material 154 as subsequent portions of the doped silicon material 154 are removed. This process can (a) eliminate the defects 156 present in the doped silicon material 154, and (b) prevent the formation of additional defects 156, as described in greater detail below.

[0022] In one embodiment, the second polishing liquid 160b is dispensed onto the polishing pad 140 via a dispense conduit 144. In one aspect of this embodiment, the second polishing liquid 160b dispensed via the dispense conduit 144 can include a surfactant and can completely displace the first polishing liquid 160a. In another aspect of this embodiment, the dispense conduit 144 can dispense a surfactant (and, optionally, other constituents) which mix with the existing first

polishing liquid 160a on the polishing pad 140 to form the second polishing liquid 160b. In still a further embodiment, described below with reference to Figure 5, the microfeature workpiece 150 can be moved from one polishing pad having the first polishing liquid 160a to a second polishing pad having the second polishing liquid 160b. In any of these embodiments, the doped silicon material 154 of the microfeature workpiece 150 is exposed to a polishing liquid having a surfactant with characteristics selected to remove and/or prevent the formation of the defects 156, as described in greater detail below.

[0023] In one embodiment, the surfactant is selected to be generally non-ionic. It is believed that a generally non-ionic surfactant can more readily adhere to an exposed surface 157 of the doped silicon material 154. Accordingly, the surfactant can passivate the exposed surface 157. This in turn can reduce the tendency for the polishing process to preferentially remove material from (a) grain boundaries of the doped silicon material 154 and/or (b) dopant-rich areas of the doped silicon material 154. In other embodiments, the generally non-ionic surfactant can reduce the number of defects 156 and/or the rate at which the defects 156 re-form via other mechanisms. In still further embodiments, the surfactant can have relatively low but non-zero ionicity while still performing these functions.

[0024] In a particular embodiment, the second polishing liquid 160b can simultaneously remove doped silicon material 154 from regions of having different crystalinities and/or different doping characteristics. Regions having different crystalinities include but are not limited to regions having different crystal orientations and/or different degrees of crystal order (e.g. different levels of amorphousness). Regions having different doping characteristics can include but are not limited to regions having different concentrations of dopants and/or different distributions of dopants. In any of these embodiments, the second polishing liquid 160b can simultaneously and uniformly remove selected quantities of the doped silicon material 154 from the microfeature workpiece 150 despite the differences in crystalinity and/or doping characteristics. For example,

the second polishing liquid 160b can remove the portions of doped silicon material 154 from different regions of the microfeature workpiece 150 at at least approximately the same rate, despite variations in crystalinity and/or doping characteristics from one region to another.

[0025] In one embodiment, the surfactant of the second polishing liquid 160b can include polyoxyethylene ether. In a particular embodiment, the surfactant can have a chemical makeup identified by CAS No. 9004-95-9 (with CAS referring to the Chemical Abstracts Service, a division of the American Chemical Society). This surfactant is also identified by the trade name "Brij 58" (owned by ICI Americas of Wilmington, Delaware). In a particular aspect of this embodiment, the second polishing liquid 160b can include Brij 58 surfactant at a concentration of about 0.001% to about 1.0% by weight. In further particular embodiments, the second polishing liquid 160b can include Brij 58 surfactant at a concentration of from about 0.1% to about 1.0%, or about 0.3% to about 1.0% by weight. In other embodiments, the surfactant can have other chemical compositions including, but not limited to, those identified in the article by Lee et al., previously incorporated herein by reference. In still further embodiments, the second polishing liquid 160b can include ionic surfactants at relatively low concentrations (e.g., less than 0.5% by weight), for example, in combination with one or more non-ionic surfactants.

[0026] One characteristic of the surfactant (in addition to reducing the likelihood for the formation and/or reformation of the defects 156) is that it can reduce the overall removal rate of the doped silicon material 154. Accordingly, it may be advantageous to limit the amount of the surfactant in the second polishing liquid 160b, for example, to a value of less than about 1.0% by weight. In other embodiments, for example, when the speed with which the doped silicon material 154 is removed is of less importance, the amount of surfactant in the second polishing liquid 160b can be increased.

[0027] In any of the foregoing embodiments, the second polishing liquid 160b can have an alkaline pH. For example, the second polishing liquid 160b can include an alkaline silica slurry having potassium hydroxide, sodium hydroxide,

tetramethyl ammonium hydroxide, and/or piperazine. In other embodiments, the second polishing liquid 160b can include other constituents that provide the appropriate pH.

[0028] In one aspect of an embodiment described above with reference to Figures 2 and 3, at least a portion of the doped silicon material 154 is removed at a relatively high rate with the first polishing liquid 160a, in a process that may tend to form the defects 156. For example, this process can include a "bulk removal" process, conducted with a first polishing liquid 160a that does not include a surfactant, or includes a low enough concentration of surfactant so as not to significantly impede the material removal rate. The defects 156 are then removed at a slower rate as additional doped silicon material 154 is chemically-mechanically polished from the workpiece 150 by the second polishing liquid 160b. An advantage of this arrangement is that the combined or overall rate at which the doped silicon material 154 is removed can be at least moderately high because the initial portion of the doped silicon material 154 can be removed at a relatively high rate. In another embodiment, the initial "bulk removal" step can be eliminated, and the entire amount of doped silicon material 154 removed from the workpiece 150 can be removed with the second polishing liquid 160b. Such a method can be used, for example, when the total amount of doped silicon material 154 to be removed is relatively small, and/or when it is less critical that the doped silicon material 154 be removed quickly, and/or when it is undesirable to form any defects 156 (even those that can be subsequently removed) in the doped silicon material 154.

[0029] Referring now to Figure 4, the doped silicon material 154 can be removed to the level of the intermediate layer 155. In one embodiment, for example, when the intermediate layer 155 includes an antireflective coating, the material removal process can include removing the intermediate layer 155 to expose the substrate material surface 152. In another embodiment, the intermediate layer 155 can include a stop layer, and the material removal process can be halted upon exposing the intermediate layer 155. In still a further embodiment, as described

above, the intermediate layer 155 can be eliminated, and the material removal process can continue through the doped silicon material 154 until the substrate material surface 152 is exposed.

[0030] In one aspect of certain embodiments described above with reference to Figures 2-4, the doped silicon material 154 is removed with one or two polishing liquids while remaining in contact with the same polishing pad material 140. In another embodiment, shown in Figure 5, a first portion of the doped silicon material 154 can be removed at a first apparatus 510a, and a second portion of the doped silicon material 154 can be removed at a second apparatus 510b. Each apparatus 510a, 510b can include a platen 520 carrying a polishing pad material 540 and a carrier 530 configured to support the microfeature workpiece 150. In one embodiment, each apparatus 510a, 510b includes a polishing pad material 540 having the same composition. In another embodiment, the polishing pad material 540 of the first apparatus 510a can be different than the polishing pad material 540 of the second apparatus 510b. In either embodiment, suitable polishing pad materials 540 are available from vendors including Rodel of Newark, Delaware. In either embodiment, the first apparatus 510a can be configured to remove material from the microfeature workpiece 150 with the first polishing liquid 160a, and the second apparatus 510b can be configured to remove material from the microfeature workpiece 150 with the second polishing liquid 160b.

[0031] One feature of an embodiment of an arrangement described above with reference to Figure 5 is that the first and second polishing liquids 160a, 160b can be kept separate from each other during processing. An advantage of this feature is that the chemical compositions of the polishing liquids can be maintained at controlled levels with relative ease. One feature of an embodiment of the arrangement described above with reference to Figures 2-4 is that the microfeature workpiece 150 need not be moved from one apparatus to another to remove the desired quantity of doped silicon material 154. An advantage of this

feature is that the likelihood for damaging the microfeature workpiece 150 during handling can be reduced.

[0032] One feature of any of the embodiments described above with reference to Figures 2-5 is that a polishing liquid having one or more surfactants with the foregoing characteristics can effectively remove defect-containing doped silicon material while reducing or eliminating the formation of additional defects as additional doped silicon material is removed. An advantage of this feature, when compared to processes performed without such surfactants, is that the yield of microfeature workpieces 150 conforming to specifications can increase, which can in turn reduce the cost for forming microelectronic devices, including memory chips.

[0033] From the foregoing, it will be appreciated that specific embodiments of the invention have been described herein for purposes of illustration, but that various modifications may be made without deviating from the spirit and scope of the invention. Accordingly, the invention is not limited except as by the appended claims.